CLAIM LISTING

This listing of claims will replace all prior versions, and listings of claims in the application:

IN THE CLAIMS

1. (previously presented) An integrated circuit (IC) comprising:

a first number of configurable elements; and

a second number of configuration control circuits, each having an output to control the configuration of one or more corresponding configurable elements, and each comprising:

a first input connected to a first configuration bit;

a second input connected to a second configuration bit; and

a select circuit to selectively provide either the first configuration bit or the second configuration bit to the one or more corresponding configurable elements in response to a select signal;

wherein a first subset of the configurable elements are controlled by the configuration control circuits and a second subset of the configurable elements are controlled by one or more configuration memory cells.

2. (original) The IC of Claim 1, wherein each of the first configuration bits is a first hardwired configuration bit.

3. (original) The IC of Claim 2, wherein each of the second configuration bits is a second hardwired configuration bit.

4. (original) The IC of Claim 3, wherein the first and second hardwired configuration bits configure the one or more corresponding configurable elements to different configuration states.

5. (original) The IC of Claim 3, wherein the first input is hardwired to a supply voltage and the second input is hardwired to ground potential.

6. (original) The IC of Claim 3, wherein the first input is hardwired to ground potential and the second input is hardwired to a supply voltage.

7. (original) The IC of Claim 3, wherein the first and second hardwired configuration bits configure the one or more corresponding configurable elements to the same configuration state.

8. (original) The IC of Claim 7, wherein the first and second inputs are hardwired to a supply voltage.

9. (original) The IC of Claim 7, wherein the first and second inputs are hardwired to ground potential.

10. (original) The IC of Claim 1, wherein the configuration control circuits do not include any memory cells.

11. (original) The IC of Claim 1, wherein the select circuit comprises a multiplexer.

12. (original) The IC of Claim 1, wherein the select circuit comprises an inverter.

13. (original) The IC of Claim 1, wherein the select circuit comprises:

a first transistor connected between the first input and the output and having a gate responsive to the select signal; and

a second transistor connected between the second input and the output and having a gate responsive to a complement of the select signal.

14. (previously presented) The IC of Claim 13, wherein the first transistor comprises an NMOS transistor and the second transistor comprises a PMOS transistor.

15. (previously presented) The IC of Claim 13, wherein the first and second transistors comprise NMOS transistors, and each configuration control circuit further comprises an inverter having an input connected to the gate of the first transistor and having an output connected to the gate of the second transistor.

16. (original) The IC of Claim 1, wherein the select signal is generated within the IC.

17. (original) The IC of Claim 1, wherein the select signal comprises an external signal provided to an input pin of the IC.

18. (canceled)

19. (previously presented) The IC of Claim 1, wherein the one or more configuration memory cells are programmed by selected ones of the configuration control circuits.

20. (original) The IC of Claim 1, wherein each of the configuration control circuits further comprises:

a configuration memory cell connected to the first input for providing the first configuration bit.

21. (original) The IC of Claim 1, further comprising:

a configuration memory cell; and

a multiplexer having a first input coupled to an output of the configuration memory cell, a second input coupled to the output of a corresponding configuration control circuit, an output coupled to a corresponding configurable element, and a control terminal to receive a mode signal.

22. (original) The IC of Claim 21, wherein the mode signal is provided to an input pin of the IC.

23. (original) The IC of Claim 21, wherein the mode signal is generated within the IC.

24. (original) The IC of Claim 21, wherein the configuration memory cell has an input terminal connected to the output of a corresponding configuration control circuit.

25. (original) The IC of Claim 1, further comprising a plurality of configuration memory cells, each coupled between corresponding configurable elements and configurable control circuits.

26. (original) The IC of Claim 1, wherein the configurable element comprises a pass gate.

27. (original) The IC of Claim 1, wherein the configurable element comprises a multiplexer.

28. (original) The IC of Claim 1, wherein the configurable element comprises a logic gate.

29. (original) The IC of Claim 1, wherein the configurable element comprises a look-up table.

30. (original) The IC of Claim 1, wherein each of the configurable control circuits further comprises one or more additional inputs each connected one or more corresponding configuration bits, wherein the select circuit selectively provides one of the first, second, or one or more configuration bits to the one or more corresponding configurable elements in response to the select signal.

31. (currently amended) An integrated circuit (IC), comprising:

one or more configurable elements; and

means for selectively providing either a first hardwired configuration bit or a second hardwired configuration bit to the one or more configurable elements in response to a select signal;

wherein the first hardwired configuration bit is hardwired to one of a supply voltage and a ground potential; and

wherein the second hardwired configuration bit is hardwired to one of the supply voltage and the ground potential.

32. (original) The IC of Claim 31, wherein the means for selectively providing does not include any memory cells.

33. (original) The IC of Claim 31, wherein the first and second hardwired configuration bits configure the one or more configurable elements to different configuration states.

34. (original) The IC of Claim 33, wherein the first hardwired configuration bit comprises a supply voltage and the second hardwired configuration bit comprises ground potential.

35. (original) The IC of Claim 31, wherein the first and second hardwired configuration bits configure the one or more configurable elements to the same configuration state.

36. (original) The IC of Claim 35, wherein the first and second hardwired configuration bits comprise a supply voltage.

37. (original) The IC of Claim 35, wherein the first and second hardwired configuration bits comprise ground potential.

38. (original) The IC of Claim 31, wherein the means for selectively providing comprises a multiplexer.

39. (original) The IC of Claim 31, wherein the means for selectively providing comprises:

a first transistor connected between the first hardwired configuration bit and the configurable element and having a gate responsive to the select signal; and

a second transistor connected between the second hardwired configuration bit and the configurable element and having a gate responsive to a complement of the select signal.

40. (original) The IC of Claim 31, wherein the select signal is generated within the IC.

41. (original) The IC of Claim 31, wherein the select signal comprises an external signal provided to an input pin of the IC.

42. (original) The IC of Claim 31, wherein a first subset of the configurable elements are controlled by the configuration control circuits and a second subset of the configurable elements are controlled by a plurality of configuration memory cells.

43. (currently amended) An integrated circuit (IC) comprising:

a first number of configurable elements; and

a second number of configuration control circuits, each having one or more outputs connected to corresponding configurable elements, and each comprising:

one or more first inputs, each connected to either a first hardwired configuration bit or to a second hardwired configuration bit;

one or more second inputs, each connected to either the first hardwired configuration bit or to the second hardwired configuration bit; and

a select circuit to selectively connect each output to either the corresponding first input or to the corresponding second input in response to a select signal;

wherein the first hardwired configuration bit is hardwired to one of a supply voltage and a ground potential; and

wherein the second hardwired configuration bit is hardwired to one of the supply voltage and the ground potential.

44. (original) The IC of Claim 43, wherein the first hardwired configuration bit comprises a supply voltage and the second hardwired configuration bit comprises ground potential.

45. (original) The IC of Claim 43, wherein the first hardwired configuration bit configures a corresponding configurable element to a first state and the second hardwired configuration bit configures the corresponding configurable element to a second state.

46. (original) The IC of Claim 43, wherein the configuration control circuits do not include any memory cells.

47. (original) The IC of Claim 43, wherein the select circuit comprises a multiplexer.

48. (currently amended) A method of selectively configuring one or more configurable elements in an integrated circuit (IC), comprising:

generating a select signal; and

selectively providing either a first hardwired configuration bit or a second hardwired configuration bit to the configurable elements in response to the select signal;

wherein the first hardwired configuration bit is hardwired to one of a supply voltage and a ground potential; and

wherein the second hardwired configuration bit is hardwired to one of the supply voltage and the ground potential.

49. (original) The method of Claim 48, wherein the first hardwired configuration bit comprises a supply voltage and the second configuration bit comprises ground potential.

50. (original) The method of Claim 48, wherein the first and second hardwired configuration bits comprise a supply voltage.

51. (original) The method of Claim 48, wherein the first and second hardwired configuration bits comprise ground potential.

52. (original) The method of Claim 48, wherein the select signal is generated within the IC.

53. (original) The method of Claim 48, wherein the select signal comprises an input signal to the IC.